

OVERVIEW OF SIRIUS' POWER SUPPLIES

6th Power Converters for Particle Accelerators

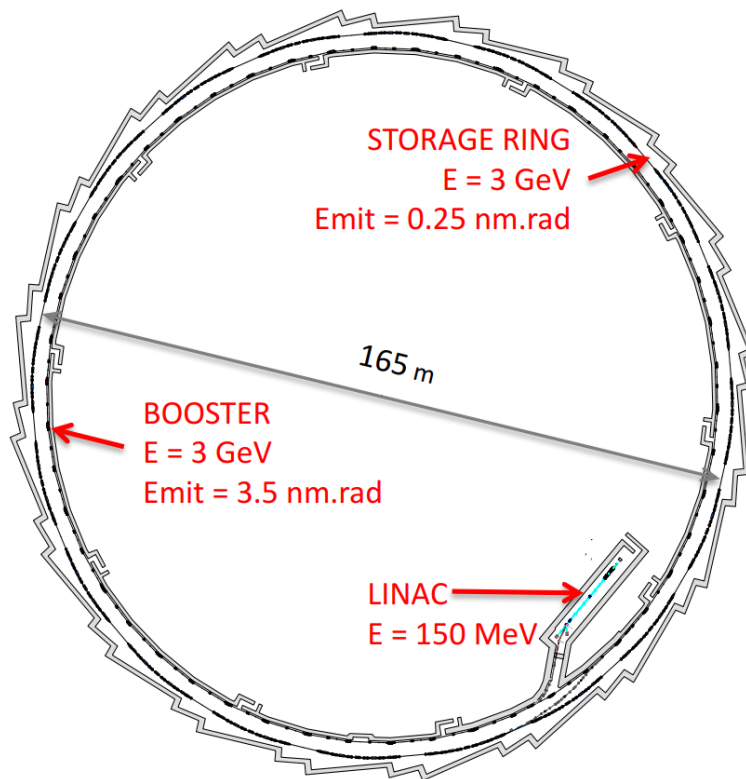
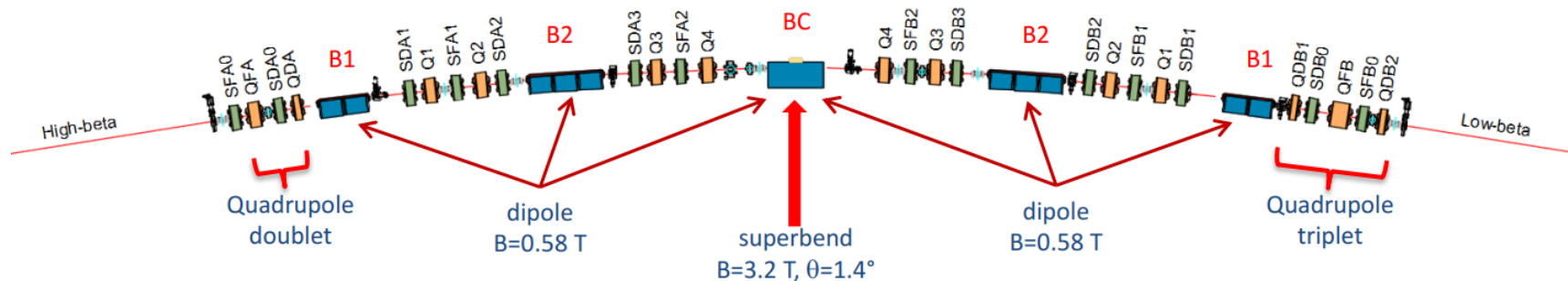
September 24th – 26th | 2018

LNLS/CNPq | Campinas - Brazil

Gabriel Oehlmeyer Brunheira

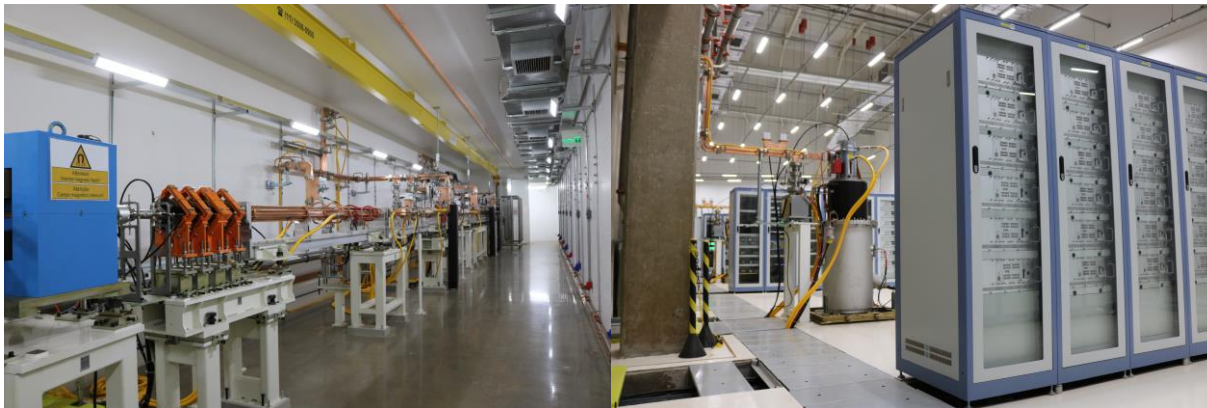
Power Electronics Group – LNLS/CNPq

- **Sirius project**
- **Power supplies families**
- **Digital controllers**
- **Production status**



Beam Energy	3.0 GeV
SR Circumference	518.4 m
Lattice	20 x 5BA
Hor. Emittance	0.25 nm.rad
Nominal current (top up)	350 mA
Booster cycling freq	2 Hz
Beamlines (1 st budget)	13

- Building construction complete, infrastructure and finishing in progress
- 150 MeV LINAC from SSRF (turn-key) installed and commissioned
- Installation of booster vacuum chamber and magnets on going
- TL's and booster PS's start in mid October



- **Effort to standardize PS's from transport lines, booster and storage rings into only three families**
 - Ease development, production and maintenance
 - Modular approach allows different combinations to fulfill all load specs

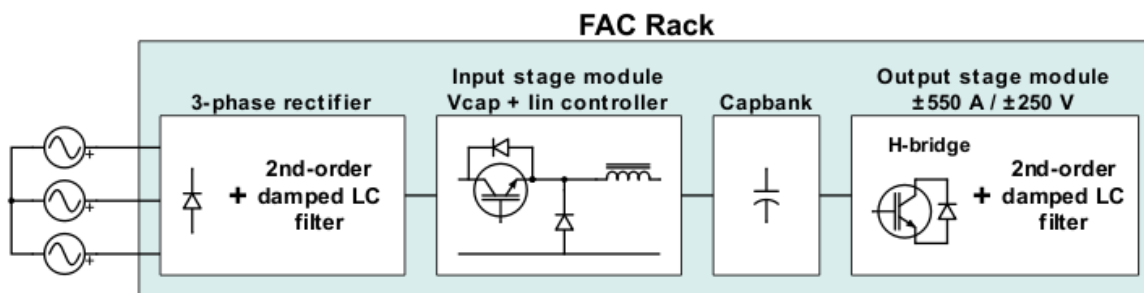
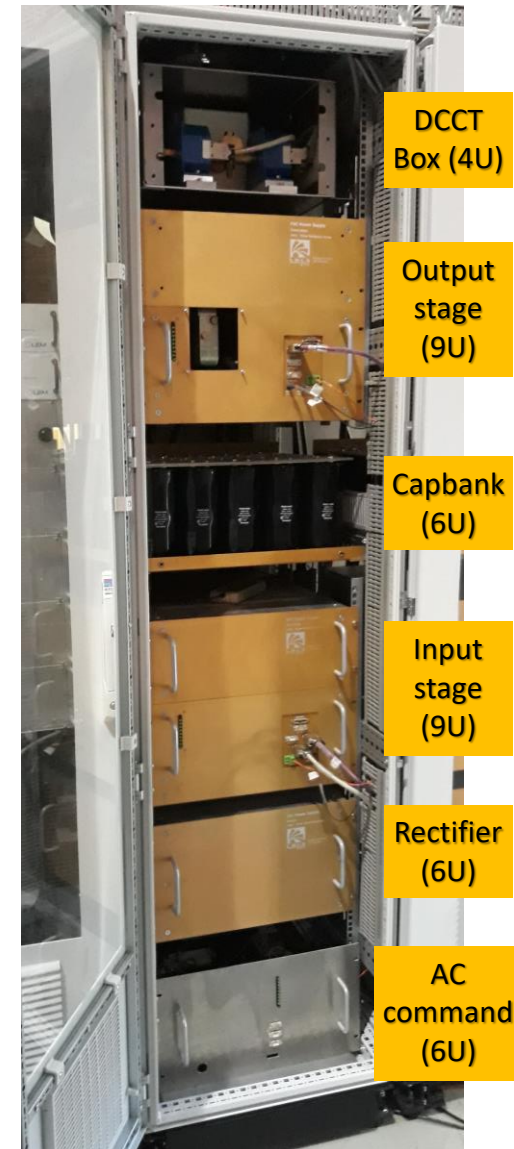
- **Converters topology:**
 - Bipolar (correctors, trim coils and booster magnets): *H-bridge + unipolar switching*
 - Unipolar (quadrupoles, sextupoles, dipoles): *Buck + coupled inductors*
 - Associated modules interleaved (lower ripple and controller delay)

PS Families	FAC AC High Power	FAP DC High Power	FBP Low Power
Module topology	IGBT Buck + Capbank + IGBT H-Bridge	Buck with Two-Interleaved IGBT	MOSFET H-Bridge
Module specs	± 550 A / 50 kW	300 A / 45 kW	± 10 A / 100 W
Power range @ Sirius	0.6 – 333.5 kW	1.5 – 180 kW	15 - 100 W
Total # of PS	6	45	732

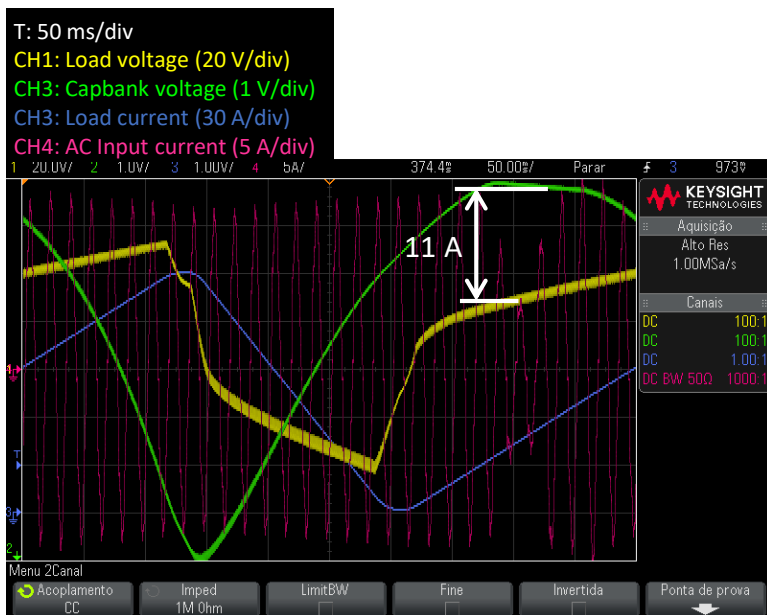
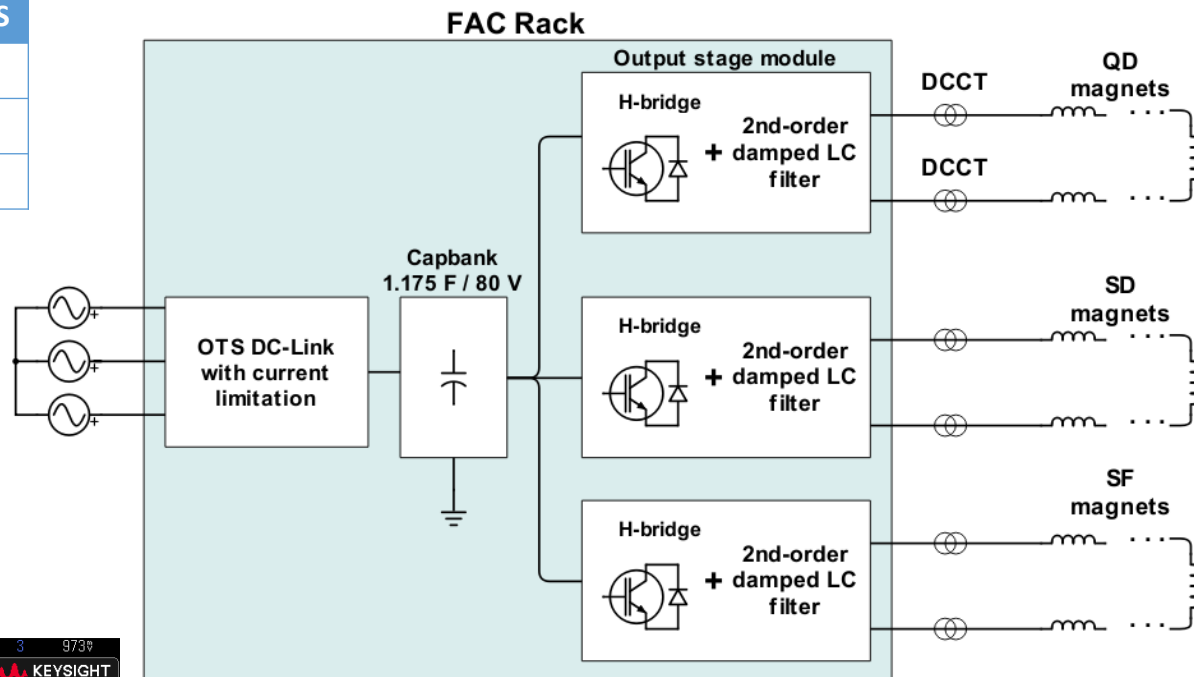
PS REQUIREMENTS

Magnets		Quadrant number	Load inductance [mH]	Load resistance [mΩ]	Nominal current [A]	Nominal voltage [V]	Nominal output power [kW]	PS model	PS Quantity		
LTB	DIPOLES		1Q	?	56.3	300	20	6	FAP	1	
	QUADRUPOLES		4Q	112.4	754.2	10	10	0.1	FBP	10	
	STEERING MAGNETS		4Q	?	354.2	10	5	0.05		11	
BTS	DIPOLES		1Q	13.8	427,125	750	35	26.25	FAP-4P	1	
	QUADRUPOLES	QF	1Q	11.6	67.03	150	10	1.5	FAP	3	
		QF/QD	1Q	6.3	55.7	150	10	1.5		5	
	STEERING MAGNETS	HORIZONTAL	4Q	3.4	423	10	5	0.05	FBP	5	
		VERTICAL	4Q	3.4	423	10	5	0.05		5	
Booster	DIPOLES		4Q	115	333.5	1000	800	333.5	FAC-2P4S	2	
	QUADRUPOLES	QF	4Q	540	2265.3	120	500	32.6	FAC-2S	1	
		QD	4Q	135	651.5	30	40	0.586	FAC	1	
	SEXTUPOLES	SF	4Q	50	253.8	150	70	5,710		1	
		SD	4Q	20	216	150	50	4,859	1		
	STEERING MAGNETS		4Q	3.4	329.2	10	5	0.05	FBP	50	
	SKEW QUADs		4Q	?	256.3	?	5	?		1	
Storage Ring	DIPOLES		1Q	316	1060.5	400	450	180	FAP-2P2S	2	
	QUADRUPOLES (Main Coils)	QFB (Q30)	1Q	348	942	160	160	25.6	FAP	1	
		QFP (Q30)	1Q	174	496.9	160	90	14.4		1	
		QFA (Q20)	1Q	116	377.1	160	70	11.2		1	
		Q1, Q2, ...(Q20)	1Q	464	1353	160	225	36		4	
		QDA, QDP1 ...	1Q	63	263.5	160	50	8		3	
		QDB1, QDB2	1Q	126	475.2	160	80	12.8		2	
	SEXTUPOLES	SDB0, SDB1, ...	1Q	116	699	160	120	19.2	FAP	7	
		SDA0, .SDA1, ...	1Q	58	375.4	160	70	11.2		14	
	QUADRUPOLES (Trim Coils)	Q30	4Q	10.7	425.4	10	5	0.05	FBP	30	
		Q20	4Q	7.2	395.4	10	5	0.05		170	
		Q14	4Q	5	415.4	10	5	0.05		70	
	STEERING MAGNETS	SLOW	Horiz.	4Q	142	378.96	10	5	0.05	FBP	120
			Vertic.	4Q	103	326.46	10	5	0.05		140
			Vertic. Ext	4Q	6.8	357.56	10	5	0.05		20
	SKEW QUADs	SLOW (Sext.)	4Q	89.6	337.06	10	5	0.05	FBP	80	
		SLOW (Fast St.)	4Q	6.32	1411.36	3	5	0.015		20	
TOTAL:									783		

- Booster high-power cycling current sources
- Water-cooled IGBT's heatsinks and inductors
- 2 Hz triangular waveform (sync @ 8 kHz)
- Suppression of AC grid oscillation:
 - **Capbank voltage control: PI + notch filters @ $2 \times n$ Hz**
 - **Input current: PI + resonant controllers @ $2 \times n$ Hz**
- Reference & capbank voltage feedforward to improve tracking error on load current



Nominal ratings	Magnets	L [mH]	# PS
30 A / 40 V	QD	135	1
150 A / 50 V	SD	20	1
150 A / 70 V	SF	50	1

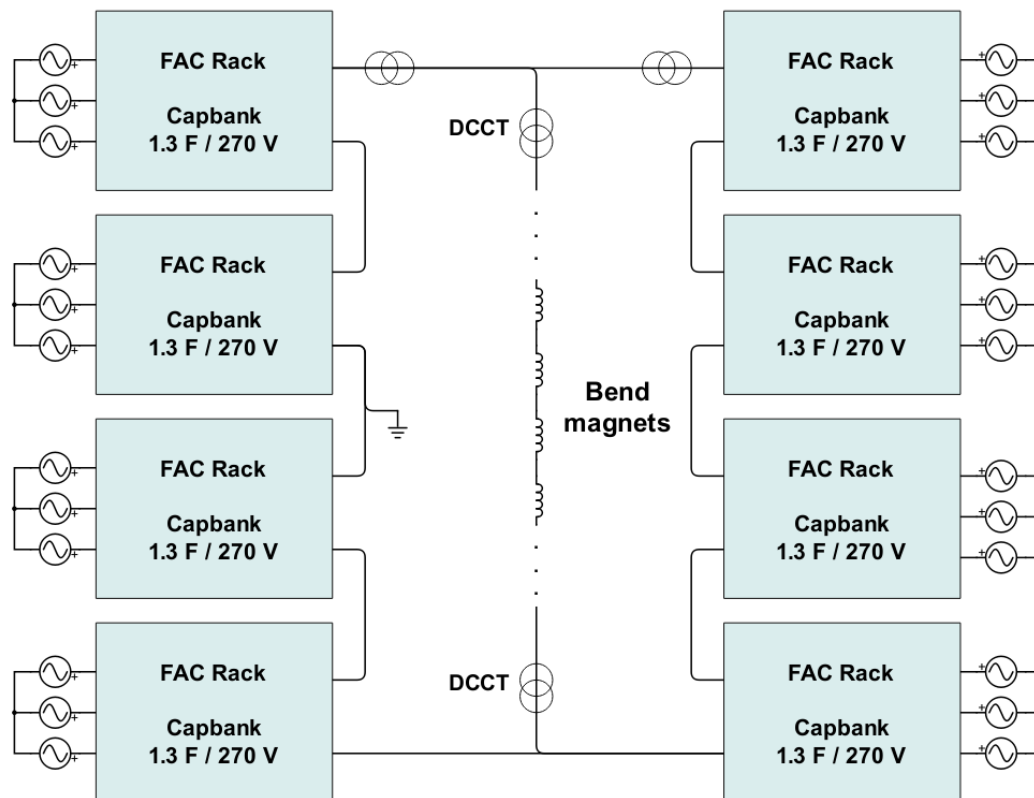
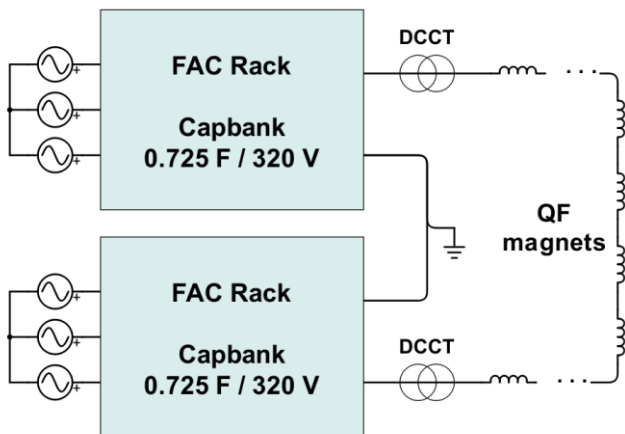


Peak load current: 150 A

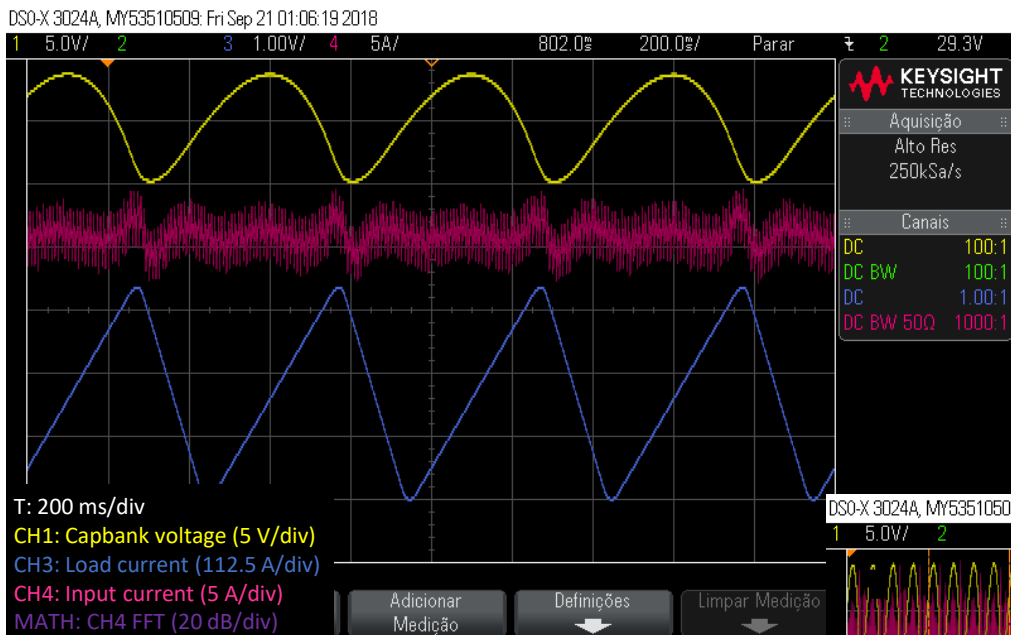
Load: 39 mH / 0.250 Ω

Capbank: 80 V_{DC} / 8 V_{pk-pk}

DC-Link current limitation: 28 A



PS Topology	Nominal ratings	Magnets	L [mH]	# PS
FAC-2S	120 A / 500 V	QF	540	1
FAC-2P4S	1100 A / 800 V	Dipoles	115	2



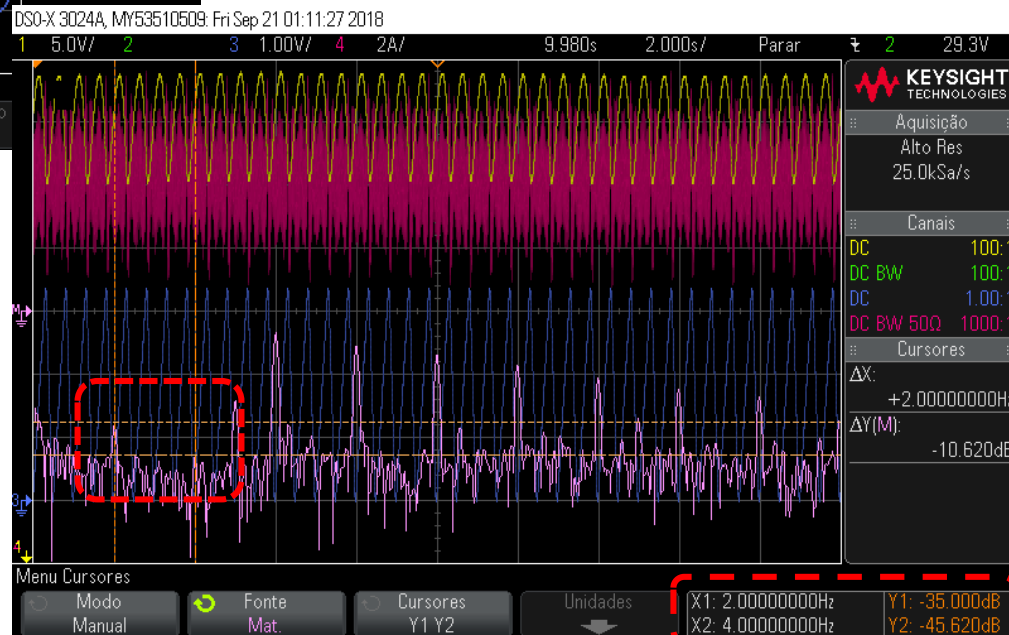
Peak load current: 380 A

Load: 11.5 mH / 0.157 Ω

Capbank: 195 V_{DC} / 8.6 V_{pk-pk}

Buck input current: 40.1 A_{DC} / 5.6 A_{pk-pk}

Notch filters and resonant controllers on 2 Hz and 4 Hz



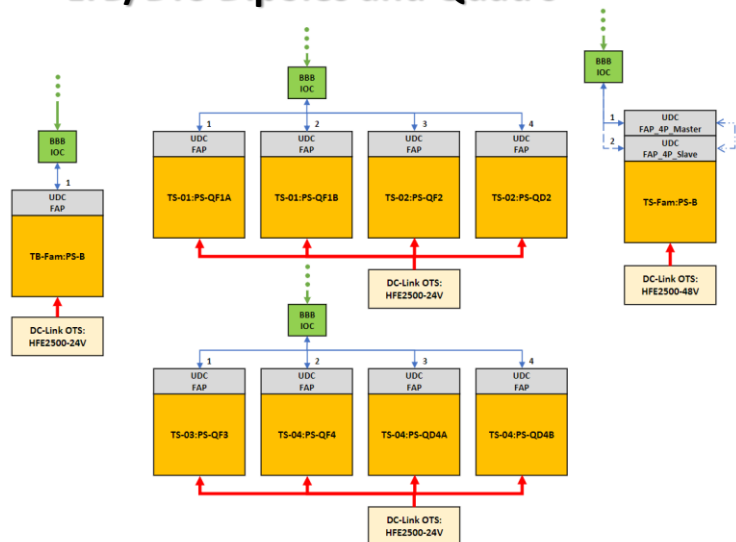
- Transport lines and storage ring high-power converters
- Buck converter with 2 interleaved IGBTs connected by coupled inductors (developed in-house).
- Water-cooled heatsink and inductors. Manifold installed inside racks to distribute between different power modules
 - *98% eff typ.*
 - *IGBT's temp: 49°C*
 - *Inductors temp: 68°C*
- Off-the-shelf adjustable DC-links optimize output stage to work at 50% duty-cycle
 - *High voltage: Regatron TopCon*
 - *Low voltage: TDK Lambda HFE*



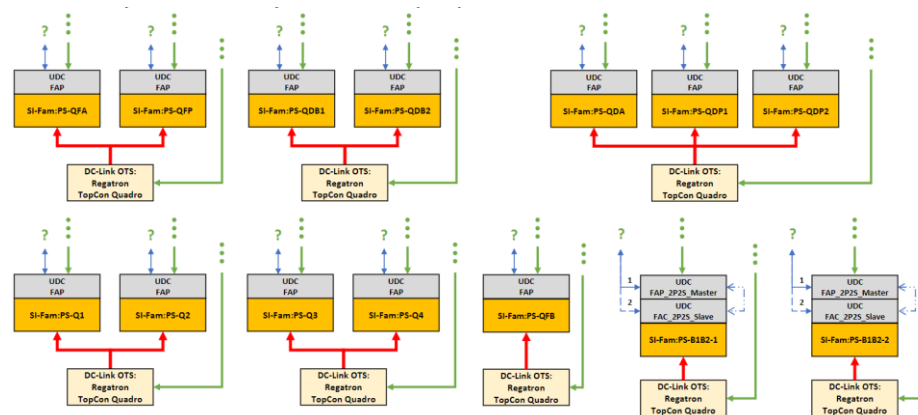
BTS Quadrupoles PS's



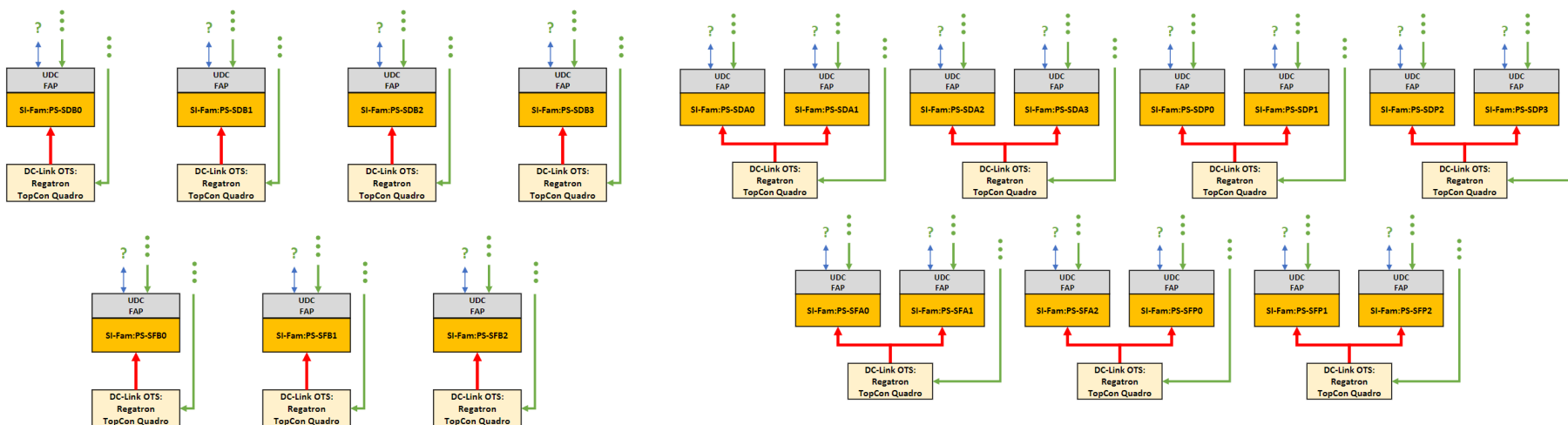
LTB/BTS Dipoles and Quad's



Storage Ring Dipoles and Quad's



Storage Ring Sextupoles



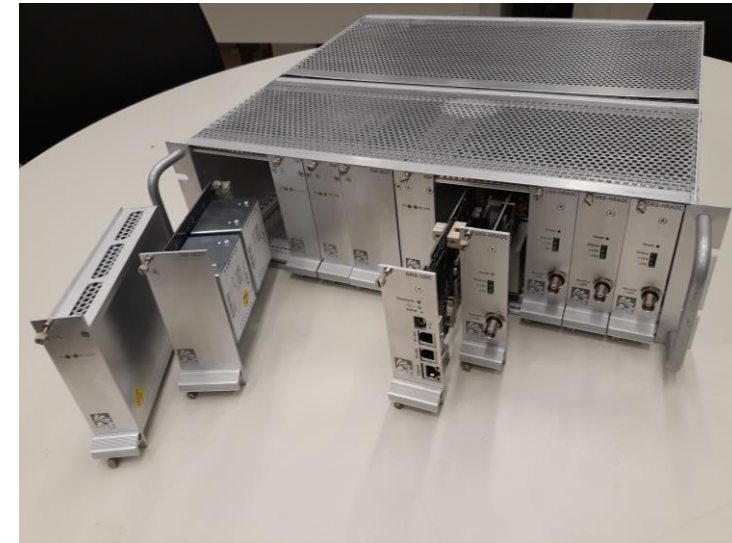
Storage Ring			Booster		LTB		BTS
Quad Trim Coils	Corrector Magnets	Skew Quad	Corrector Magnets	Skew Quad	Quad	Corrector Magnets	Corrector Magnets
270	280	100	50	1	10	11	10

- 3U crate houses up to 4 individual ± 10 A / ± 10 V
 - Air-cooled forced by rack exhaustor (except TL)
 - > 4 kHz bandwidth

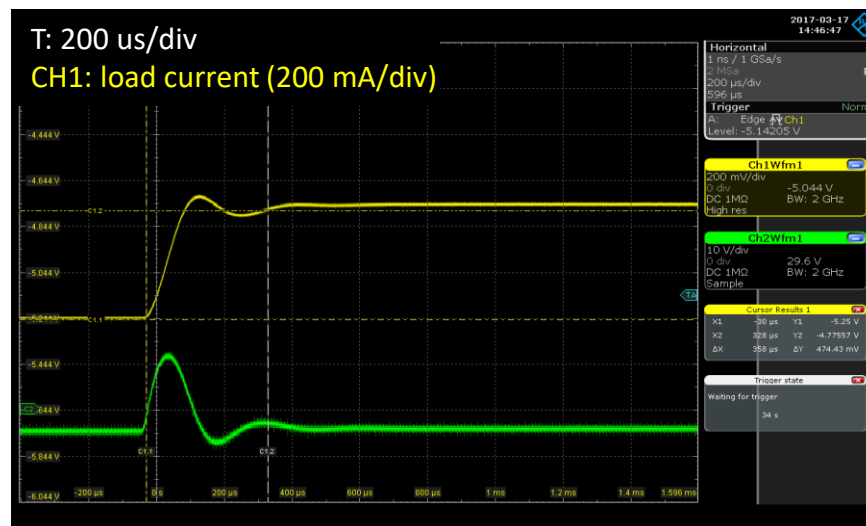
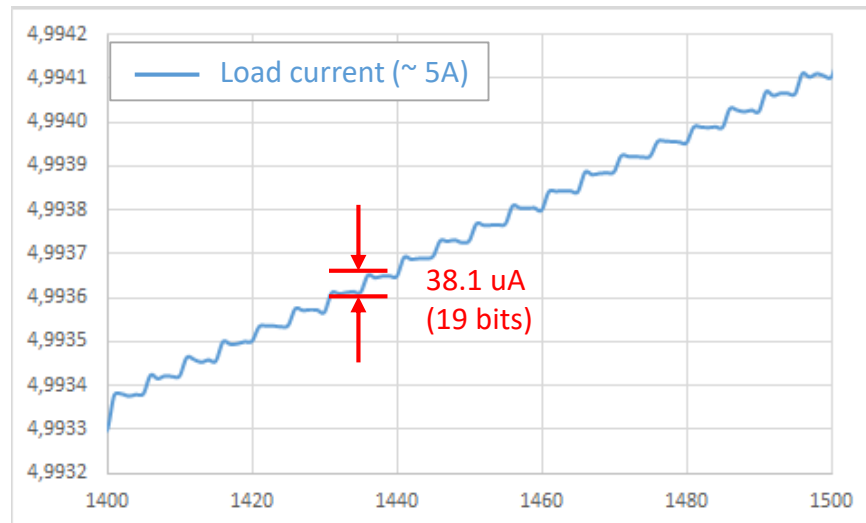
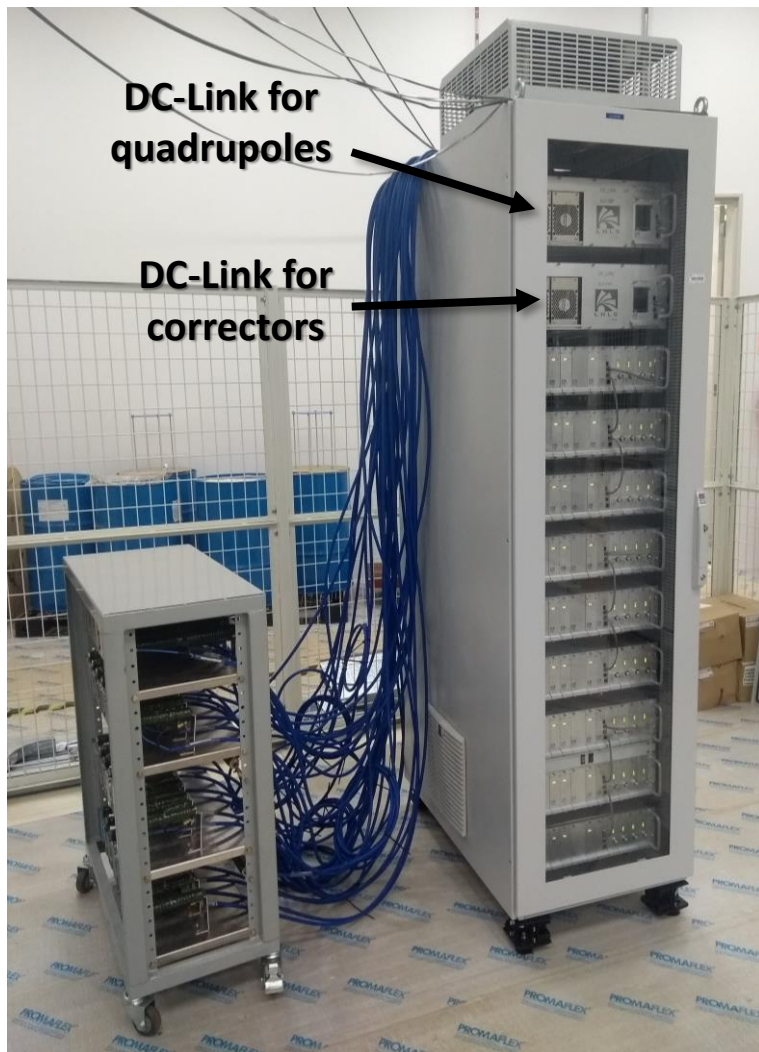
- MOSFETs H-Bridge ($f_{\text{PWM}} = 50$ kHz) + 2nd order LC-damped filter - 89% eff typ.

- Off-the-shelf AC/DC converters for shared DC-link among crates from same rack (adjustable for different set of loads)

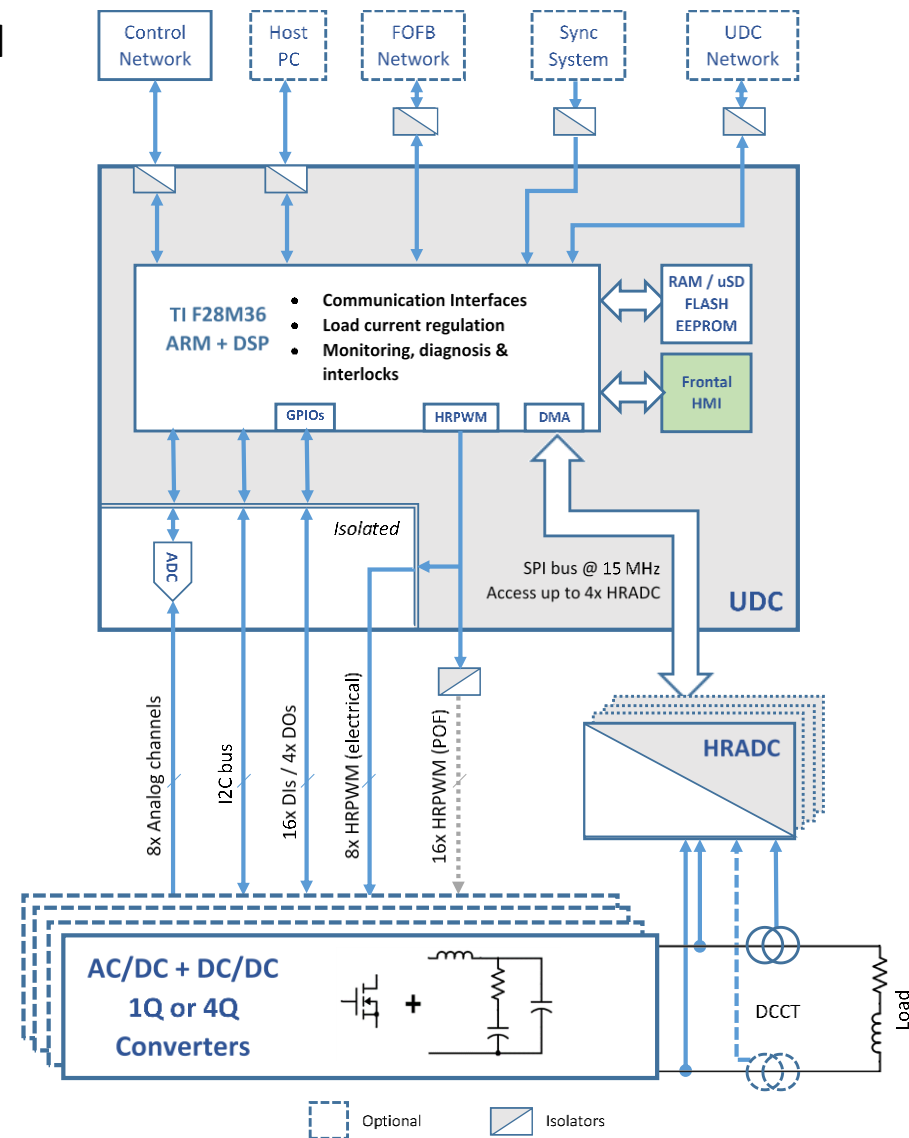
- First prototypes installed at UVX's LINAC two years ago and 10 units of final version installed this year. FBP rack for TL's already in place at Sirius



LTB/BTS FBP power supplies



- 3U based in-house development, with initial partnership with University of Campinas
- UDC (Universal Digital Controller):
 - *Dual-core TI F28M36P63C2: ARM + DSP*
 - *Up to 4 indepen. PI controllers @ 100 kHz*
- HRADC (High-Resolution A/D Converter):
 - *18 bits @ up to 600 kSPs*
 - *Voltage / current input (Vishay VPR burden)*

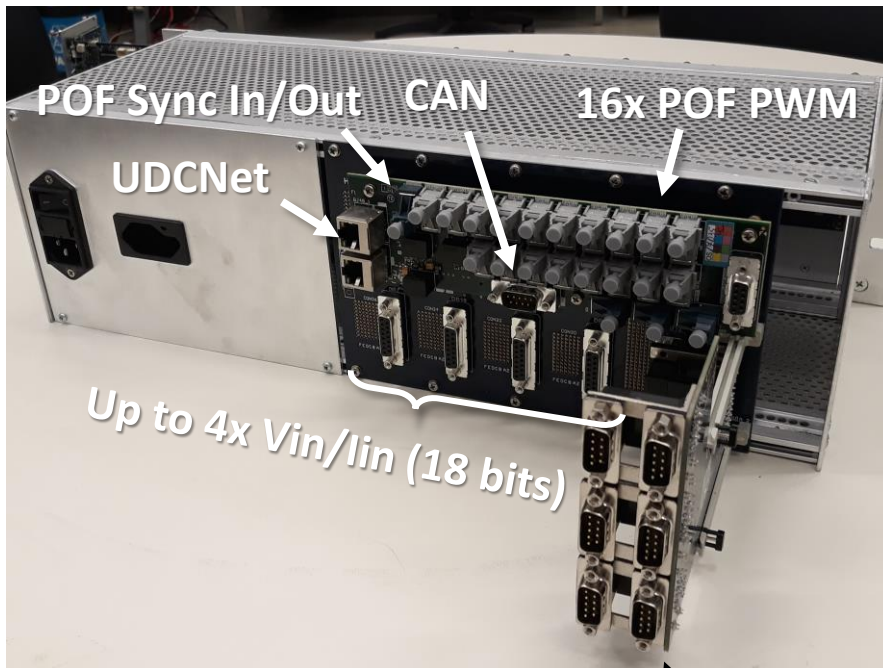




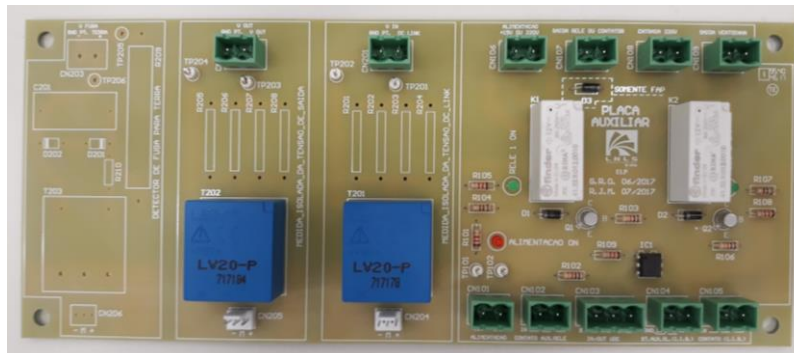
Interlock board (CAN with UDC)



25/09/2018



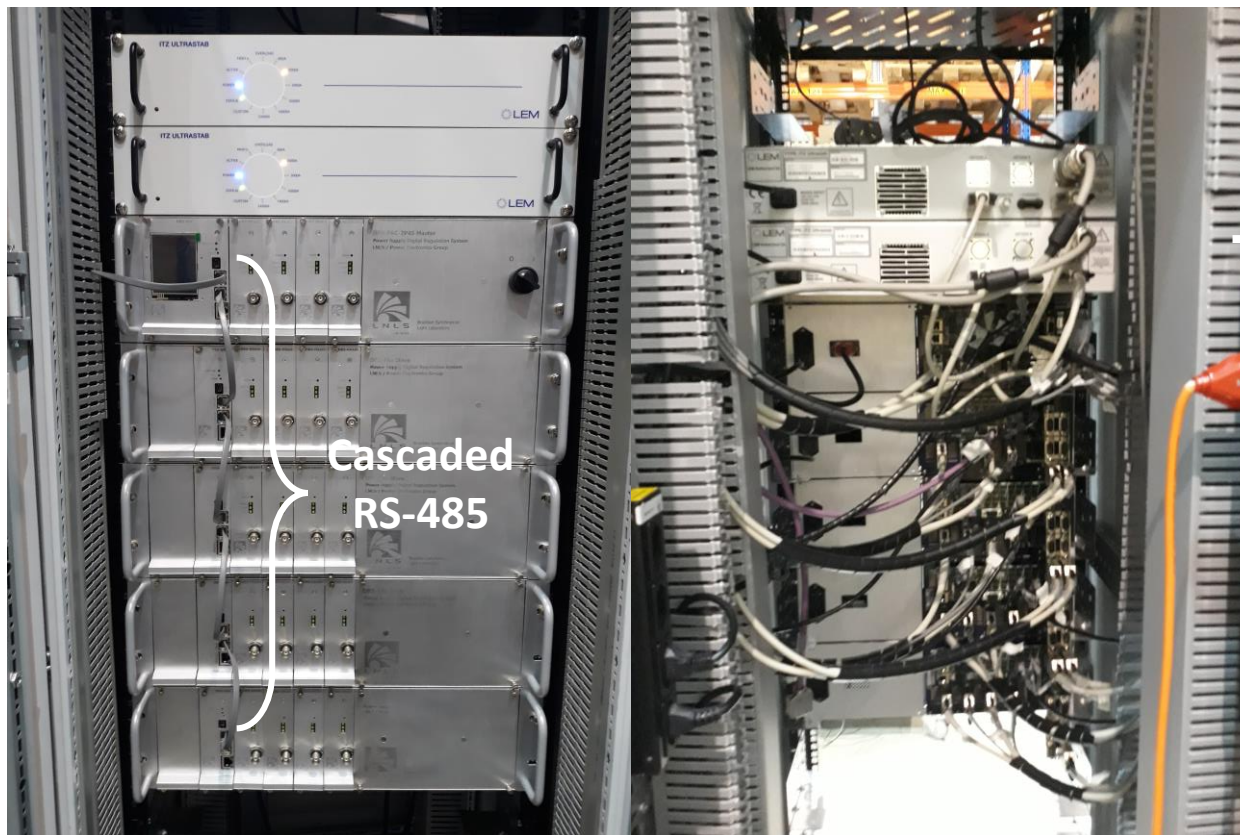
Auxiliary board (AC contactor/relays, isolations, etc)



Overview of Sirius' Power Supplies – 6th POPCA

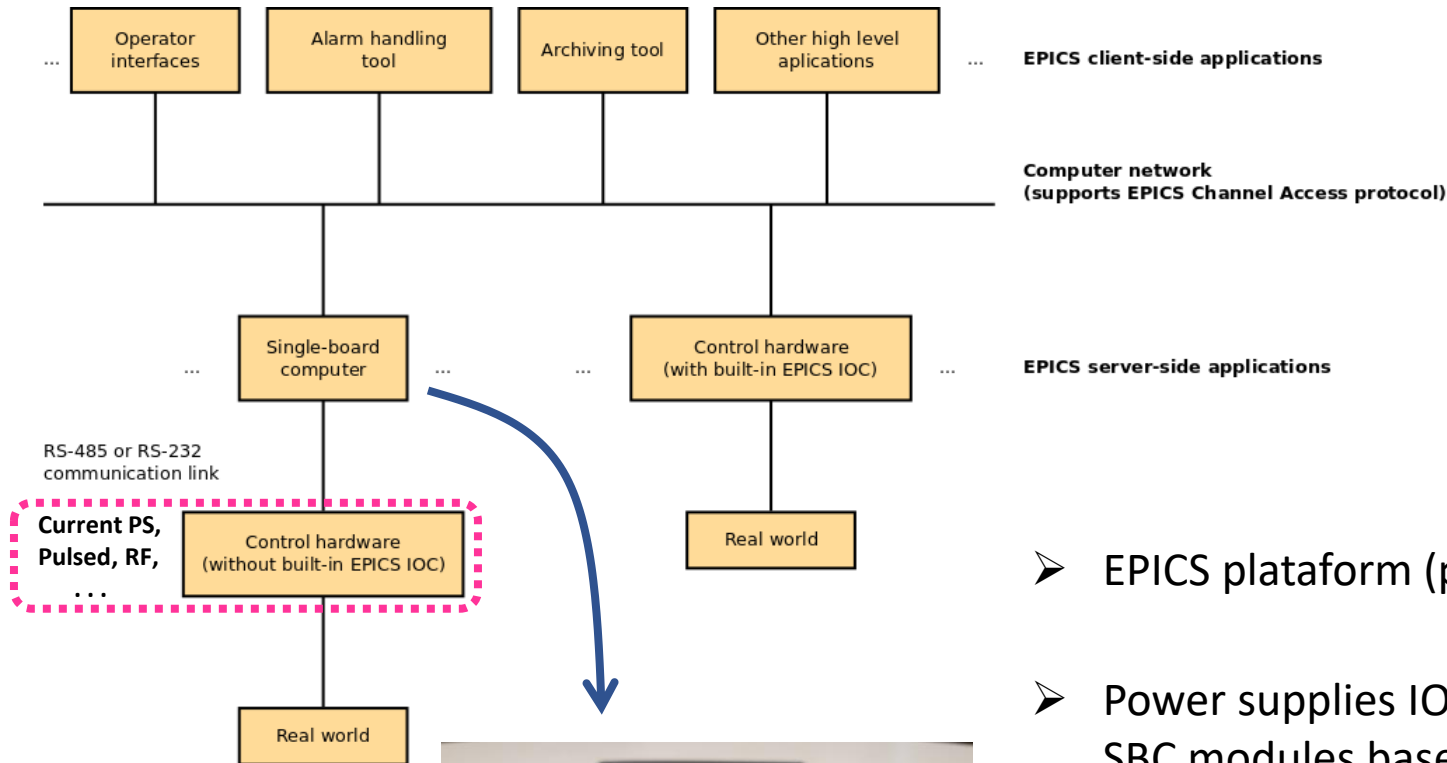
Expansion board with isolated AIN + DI/O's from/to multiple PS power stages

Booster Dipole Controller



LTB/BTS PS Controllers





- EPICS platform (pydm, CCS, ...)
- Power supplies IOC's implemented on SBC modules based on BeagleBone Black:
 - RS-485 @ 6Mbps
 - BSMP protocol (in-house)
 - Synchronization by serial interface, instead on direct pulses

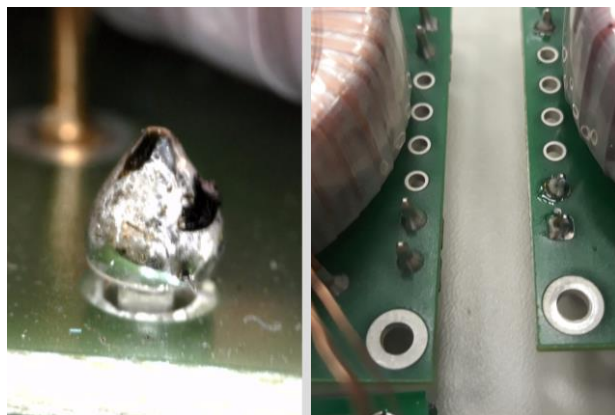


- FAC
 - 100% modules manufactured, ~90% tested
 - Racks integration and tests in progress

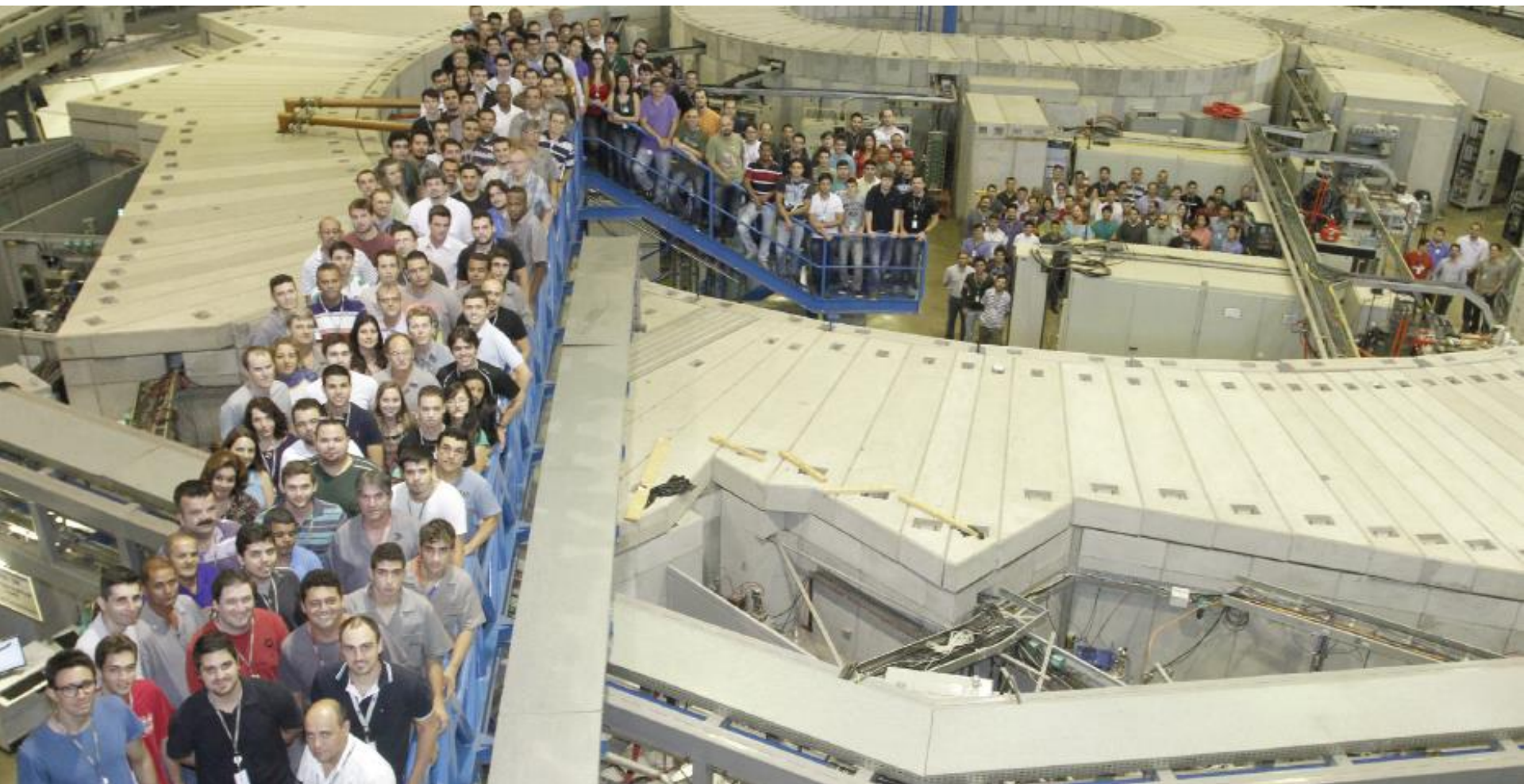
- FAP
 - 100% modules manufactured
 - All LTB/BTS modules tested, racks integration finish on next fews days

- FBP
 - 1 rack (LTB/BTS) installed and operating with dummy loads
 - 380 power supplies (95 crates) delivered and tested – sufficient for Sirius operation without trim coils and QS
 - DCCTs recall (~50% !!)

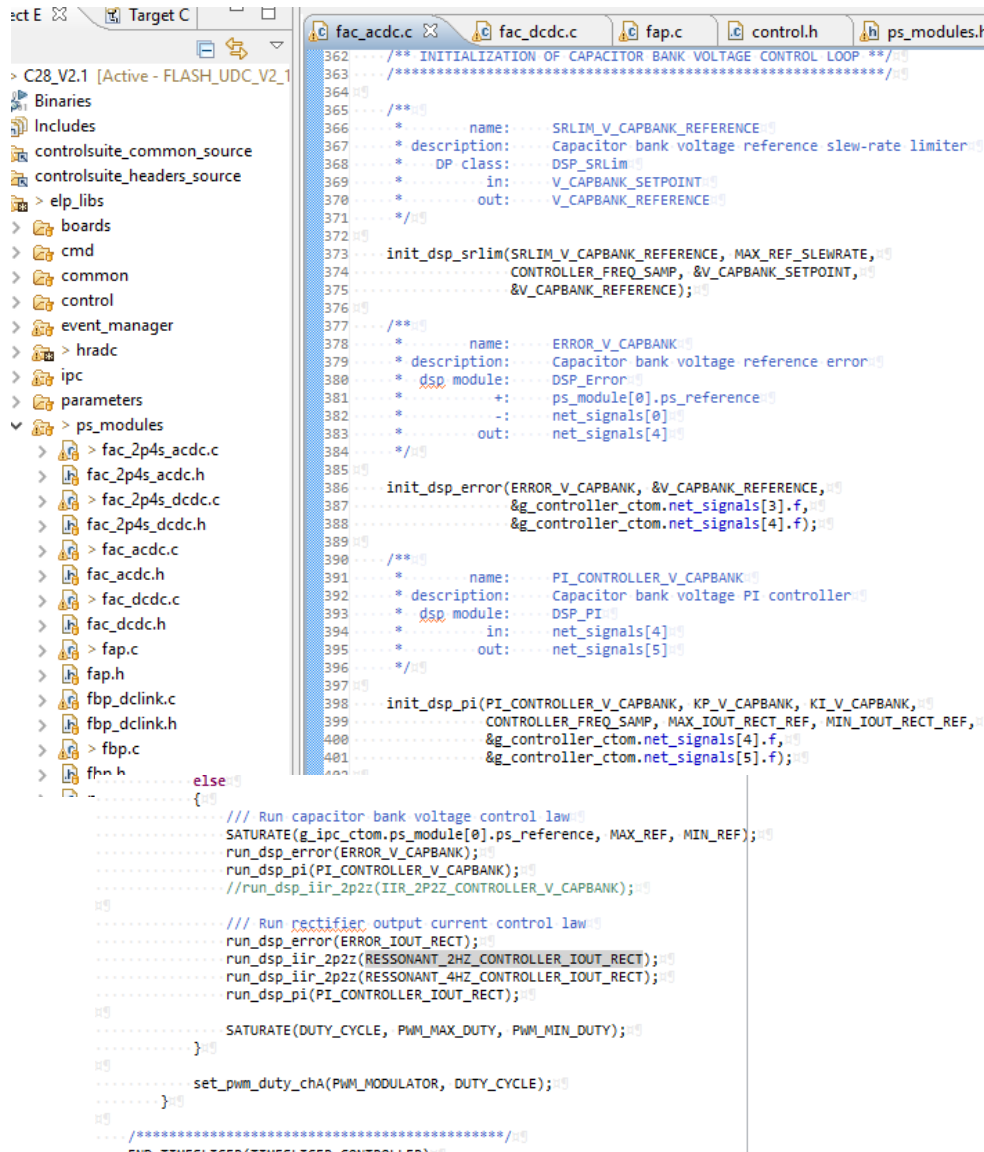
- DRS (FAC/FAP)
 - > 90% electronics completed (in-house HW customization)
 - LTB, BTS and Booster PS controllers assembled, under tests
 - Cabling and rack integration on going
 - Firmware in progress







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```

362  /** INITIALIZATION OF CAPACITOR BANK VOLTAGE CONTROL LOOP **/
363  /*******
364
365  /**
366  *   name:     SRLIM_V_CAPBANK_REFERENCE
367  *   description: Capacitor bank voltage reference slew-rate limiter
368  *   DP class:  DSP_SRLim
369  *   in:       V_CAPBANK_SETPOINT
370  *   out:      V_CAPBANK_REFERENCE
371  */
372
373  init_dsp_srlim(SRLIM_V_CAPBANK_REFERENCE, MAX_REF_SLEWRATE,
374               CONTROLLER_FREQ_SAMP, &V_CAPBANK_SETPOINT,
375               &V_CAPBANK_REFERENCE);
376
377  /**
378  *   name:     ERROR_V_CAPBANK
379  *   description: Capacitor bank voltage reference error
380  *   dsp module: DSP_Error
381  *   ps module: ps_module[0].ps_reference
382  *   net signals: net_signals[0]
383  *   out:      net_signals[4]
384  */
385
386  init_dsp_error(ERROR_V_CAPBANK, &V_CAPBANK_REFERENCE,
387               &g_controller_ctom.net_signals[3].f,
388               &g_controller_ctom.net_signals[4].f);
389
390  /**
391  *   name:     PI_CONTROLLER_V_CAPBANK
392  *   description: Capacitor bank voltage PI controller
393  *   dsp module: DSP_PI
394  *   in:       net_signals[4]
395  *   out:      net_signals[5]
396  */
397
398  init_dsp_pi(PI_CONTROLLER_V_CAPBANK, KP_V_CAPBANK, KI_V_CAPBANK,
399             CONTROLLER_FREQ_SAMP, MAX_IOUT_RECT_REF, MIN_IOUT_RECT_REF,
400             &g_controller_ctom.net_signals[4].f,
401             &g_controller_ctom.net_signals[5].f);
402
403  else
404  {
405      /** Run capacitor bank voltage control law
406      .....
407      SATURATE(g_ipc_ctom.ps_module[0].ps_reference, MAX_REF, MIN_REF);
408      run_dsp_error(ERROR_V_CAPBANK);
409      run_dsp_pi(PI_CONTROLLER_V_CAPBANK);
410      //run_dsp_iir_2p2z(IIR_2P2Z_CONTROLLER_V_CAPBANK);
411      .....
412      /** Run rectifier output current control law
413      run_dsp_error(ERROR_IOUT_RECT);
414      run_dsp_iir_2p2z(RESSONANT_2HZ_CONTROLLER_IOUT_RECT);
415      run_dsp_iir_2p2z(RESSONANT_4HZ_CONTROLLER_IOUT_RECT);
416      run_dsp_pi(PI_CONTROLLER_IOUT_RECT);
417      .....
418      SATURATE(DUTY_CYCLE, PWM_MAX_DUTY, PWM_MIN_DUTY);
419      .....
420      }
421      set_pwm_duty_cha(PWM_MODULATOR, DUTY_CYCLE);
422      .....
423  }
424  /*******
425  END THE CONTROL LOOP
  
```

- One project/core to maintain (Git)
- New PS models require only 2 files:
 - *new_model.c* (source)
 - *new_model.h* (header)
- Completely parameterized
 - PWM settings (freq/dead-time/sat)
 - Communication settings
 - Control parameters
 - Interlocks thresholds
 - # PS (FBP only)
 - ...
- Control laws are built and run 'blockwise' inside each PS module

